

ABSTRACT OF THE DISCLOSURE

An input/output buffer. An input/output circuit is composed of a first PMOS transistor and a first NMOS transistor, has an I/O port coupled to an I/O pad, and a N-well region. An N-well control circuit controls the voltage level at the N-well region of the first PMOS transistor according to input signals at the I/O pad. A P-gate control circuit receives a second gate control signal and outputs to the gate of the first PMOS transistor. The P-gate control circuit is composed of a transmission gate and a third PMOS transistor. The transmission gate and the third PMOS transistor do not have to follow the design rule for ESD, and the wafer area required for the P-gate control circuit can be decreased because the P-gate control circuit is not directly connected to the I/O pad.